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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,542	09/30/2003	Moo Jin Lee	049128-5127	1841

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EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,542	LEE ET AL.	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5,6,18-20 and 22-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6,18-20 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 18-20 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) and Nanno (US 6,909,413).

Regarding **Claim 5**, the AAPA teaches a method for supplying power to a liquid crystal display comprising steps of:

taking a power source greater than 3.0V from a system (AAPA, Fig. 2); and

supplying the power source voltage to digital circuit devices including a data driving circuit, and a gate driving circuit for processing digital signal with respect to a reference voltage provided from a DC-DC converter (AAPA, Fig. 2 Vcc, Vdd, VGH, VGL and Vcom).

The AAPA fails to teach that the power source is less than 3.0V. Nanno teaches a similar power source used for the same function that is 1.8V (Nanno, Figs. 2 and 4 VDD). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power supply of Nanno in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 6**, the AAPA further teaches that the DC-DC converter is used for raising or reducing the power source voltage from the system to generate reference voltages to be supplied to the liquid crystal panel (AAPA, Pg. 2 paragraph [0013]).

Regarding **Claim 18**, the AAPA teaches an apparatus for supplying power to a liquid crystal display comprising steps of:

a system for generating a power voltage over 3.0V (AAPA, Fig. 2); and

digital circuit devices including a data driving circuit, and a gate driving circuit for processing digital signal with respect to a reference voltage provided from a DC-DC converter by taking the power voltage (AAPA, Fig. 2 Vcc, Vdd, VGH, VGL and Vcom).

The AAPA fails to teach that the power source is under 3.0V. Nanno teaches a similar power source used for the same function that is 1.8V (Nanno, Figs. 2 and 4 VDD). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power supply of Nanno in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 19**, the AAPA further teaches that the DC-DC converter is used for raising or reducing the power source voltage from the system to generate reference voltages to be supplied to the liquid crystal panel (AAPA, Pg. 2 paragraph [0013]).

Regarding **Claim 20**, that the digital circuit device further includes:

an interface circuit for receiving a synchronous signal, a clock signal and digital video data from the system (AAPA, Fig. 2 element 11);

a timing controller for controlling the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit (AAPA, Fig. 2 element 12),

wherein the data driving circuit supplies the digital video data to the liquid crystal panel and the gate driving circuit supplies a scan pulse to the liquid crystal panel (AAPA Fig. 2 elements 13-15).

Regarding **Claim 27**, the AAPA teaches a method for supplying a power to a liquid crystal display, having digital circuit devices including an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, (AAPA, Fig. 2) comprising the steps of:

providing a first power source voltage from a system wherein the first power source voltage is 3.3V and is used to process digital signal of the digital circuit devices (AAPA, Figs. 2 and 4);

generating second power source voltages from the first power source voltage using a DC-DC converter, the second power source voltages being used as reference voltages of the digital circuit devices (AAPA, Fig. 4 DC-DC converter); and

supplying the first power source voltage and the second power source voltages to the digital circuit devices (AAPA, Fig. 4 elements 11-14).

The AAPA fails to teach that the power source is lower than 3.0V. Nanno teaches a similar power source used for the same function that is 1.8V (Nanno, Figs. 2 and 4 VDD). It would have been obvious to one of ordinary skill in the art at the time of the

invention to use the power supply of Nanno in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 28**, the AAPA further teaches that the first power source voltage is supplied to the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit (AAPA, Fig. 4 elements 11-14).

Regarding **Claim 29**, the AAPA further teaches that the second power source voltages include a VDD voltage, a VGH voltage, and a VGL voltage (AAPA, Fig. 4).

Regarding **Claim 30**, the AAPA further teaches that the VDD voltage is supplied to the data driving circuit (AAPA, Fig. 4).

Regarding **Claim 31**, the AAPA further teaches that the VGH and the VGL voltages are supplied to the gate driving circuit (AAPA, Fig. 4).

Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA in view of Tsutsui (US 7,196,701).

Regarding **Claim 22**, the AAPA teaches a method for supplying a power to a liquid crystal display, having digital circuit devices including an interface circuit, a timing controller, a data driving circuit and a gate driving circuit for processing digital signal, (AAPA, Figs. 2 and 4) comprising the steps of:

providing a first power source voltage from a system wherein the first power source voltage is over 3.0V (AAPA, Figs. 2 and 4 VCC);

the first power source voltage being used to process digital signal of the digital circuit devices (AAPA, Figs. 2 and 4 VCC elements 11-14);

generating third power source voltages from the first power source voltage using a DC-DC converter, the third power source voltages being used as reference voltages of the digital circuit devices (AAPA, Fig. 4 element 16 DC-DC converter); and

supplying the first power source voltage and the third power source voltages to the digital circuit devices (AAPA, Figs. 2 and 4 elements 11-14).

The AAPA fails to teach a second power source voltage as claimed. Tsutsui teaches a second power source voltage generated from the first power source voltage using a reducing circuit, the second power source voltage being used to process digital signal of the digital circuit devices and lower than the first power source voltage, and supplying the second power source voltage to the digital circuit devices Tsutsui Figs. 2 and 7 VDD2 is supplied as driving circuitry). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the reducing circuit as taught by Tsutsui in the display power system of the AAPA in order to provide a power saving mode.

Regarding **Claim 23**, the AAPA in view of Tsutsui further teaches that the second power source voltage is supplied to the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit (AAPA, Fig. 4 elements 11-14 and Tsutsui Figs. 2 and 7 VDD2).

Regarding **Claim 24**, the AAPA further teaches that the third power source voltages include a VDD voltage, a VGH voltage, and a VGL voltage (AAPA, Fig. 4).

Regarding **Claim 25**, the AAPA further teaches that the VDD voltage is supplied to the data driving circuit (AAPA, Fig. 4).

Regarding **Claim 26**, the AAPA further teaches that the VGH and the VGL voltages are supplied to the gate driving circuit (AAPA, Fig. 4).

Response to Arguments

Applicant's arguments with respect to claims 5, 6, 18-20, 22-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 29, 2008 - kx -

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER